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GP 2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/054,653	Confirmation No.:	9448
First Named Inventor:	Bulucea, Constantin	Filing Date:	18 January 2002
Group Art Unit:	2814	Examiner:	Farahani, D.
Atty. Docket No.:	NS-5127 US		
Title:	Gate-Enhanced Junction Varactor With Gradual Capacitance Variation		
Assignee(s):	National Semiconductor Corporation		

Mountain View, California
11 June 2004

MAIL STOP NON-FEE AMENDMENT
COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT

Sir:

Responsive to the Office Action mailed 12 February 2004, please amend the above patent application in the following manner.

IN THE SPECIFICATION

Amend paragraphs 52, 58, 86, 89, 94, 110, 117, 146, 151, 155, 165, 167, 168, 181 - 183, 194, 196, 217, 225, 226, 243, 268, 272, 279, 280, 312, and 317 as follows:

[0052] Fig. 18 is a cross-sectional plan view of an n-channel silicon-gate ~~silicon-gate~~ gate-enhanced junction varactor configured according to the invention.

[0058] Fig. 24 is a graph of varactor width-wise lineal capacitance as a function of plate-to-body voltage for the computer-simulated ~~computer-simulated~~ varactor of Fig. 22 at various constant values of gate-to-body voltage.

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